regions are exaggerated for clarity. Like reference characters and/or numerals in the drawings denote like elements, and thus their description may not be repeated.

[0024] A macroblock may refer to a unit, which composes at least a part of a frame in image processing. The macroblock may include a plurality of pixels. The macroblock may include a plurality of sub-blocks. A block herein may refer to the macroblock.

[0025] A current block herein may refer to a macroblock on which current image processing is performed. According to example embodiments, the number of sub-blocks included in the macroblock may be changed, and the number of pixels included in the macroblock may also be changed. In addition, a current frame herein may refer to a frame including the current block, and a previous frame may refer to a frame in which image processing is performed before or immediately before the current frame is image-processed.

[0026] It is assumed that a macroblock may include 16×16 pixels, that is, 16 horizontal pixels and 16 vertical pixels. Each of sub-blocks included in the macroblock includes 8×8 pixels, that is, 8 horizontal pixels and 8 vertical pixels.

[0027] For the purposes of convenience of description, a block may be expressed by a matrix. That is, a $(i,j)^{th}$ block B(i,j) herein may refer to a block positioned in an i^{th} row and a j^{th} column among a plurality of blocks. The expression manner as described above is used not only to represent a block itself but also to represent the following characteristics of the block: (i) a $(i,j)^{th}$ quantization parameter offset QPOFF(i,j) of the block, (ii) a $(i,j)^{th}$ region of interest ROI(i,j) of the block, (iii) a $(i,j)^{th}$ activity ACT(i,j) of the block, (iv) a $(i,j)^{th}$ reference quantization parameter QPREF (i,j) of the block, (iv) a $(i,j)^{th}$ lock mode LM(i,j) of the block, and (v) a $(i,j)^{th}$ quantization parameter QP(i,j) of the block. Here, i and j are natural numbers and i may or may not be equal to j.

[0028] Neighboring blocks of a current block herein may refer to a block on a left side of the current block, a block on a upper side of the current block, a block on a upper left side of the current block, and a block on a upper right side of the current block.

[0029] For example, when a current block is the $(i,j)^{th}$ block B(i,j), neighboring blocks of the current block may be a $(i-1,j-1)^{th}$ block B(i−1,j−1), a $(i-1,j)^{th}$ block B(i−1,j), a $(i-1,j+1)^{th}$ block B(i−1,j+1), and a $(i,j-1)^{th}$ block B(i,j−1).

[0030] According to example embodiments, some of blocks included in the neighboring blocks may not be present. For example, when a current block is positioned at the far most right side of a frame, a block on the upper right side among the neighboring blocks may not be present.

[0031] FIG. **1** is a block diagram of a rate controller according to example embodiments of inventive concepts.

[0032] Referring to FIG. **1**, a rate controller **100** may include at least an activity masking circuit **120** and a false negative detection circuit **140**.

[0033] The activity masking circuit **120** may receive a brightness value Y of each of pixels included in a block, and further determine a quantization parameter offset QPOFF using the received brightness value Y.

[0034] The false negative detection circuit **140** may receive the quantization parameter offset QPOFF and a reference quantization parameter QPREF, and determine a quantization parameter QP of a current block using the quantization parameter offset QPOFF and the reference quantization parameter QPREF.

[0035] FIG. **2** is a block diagram of the activity masking circuit **120** shown in FIG. **1**, FIG. **3** represents a block and sub-blocks included in the block, and FIG. **4** is a table representing strength corresponding to an average activity of a previous frame.

[0036] Referring to FIG. **2**, the activity masking circuit **120** may include at least an activity decision circuit **200**, an activity average decision circuit **300**, and an offset decision circuit **400**. The activity decision circuit **200** may include at least a variance decision circuit **220**, a comparator **240**, and a variance register **260**.

[0037] Referring to FIGS. **2** and **3**, it is assumed that a current block includes four sub-blocks. The variance decision circuit **220** may receive brightness values of pixels included in four sub-blocks SUB1, SUB2, SUB3, and SUB4.

[0038] The variance decision circuit **220** may calculate a first variance value VAR(Y1) of brightness values of pixels included in a first sub-block SUB1, calculate a second variance value VAR(Y2) of brightness values of pixels included in a second sub-block SUB32, calculate a third variance value VAR(Y3) of brightness values of pixels included in a third sub-block SUB3, and calculate a fourth variance value VAR(Y4) of brightness values of pixels included in a fourth sub-block SUB4.

[0039] The variance decision circuit **220** may sequentially transmit each result VAR(Yk) of the calculations to the comparator **240**, where k is a natural number less than or equal to 4.

[0040] The comparator **240** may receive each result VAR (Yk) of the calculations from the variance decision circuit **220**, and read a variance value VAR(Yl) stored in the variance register **260**, where l is a natural number less than or equal to 4. The comparator **240** may determine the smallest value among the variance value VAR(Yl) stored in the variance register **260**, and thereafter store the determined variance value in the variance register **260**.

[0041] For example, when a first variance value VAR(Y1) is received by the comparator **240**, the comparator **240** may store the first variance value VAR(Y1) in the variance register **260** as VAR (Yl). When a second variance value VAR(Y2) is received by the comparator **240**, the comparator **240** may read the first variance value VAR(Y1) from the variance register **260**, compare the second variance value VAR(Y2) with the first variance value VAR(Y1), and store the smaller of the second variance value VAR(Y2) and the first variance value VAR(Y1) in the variance register **260** as VAR (Yl). A comparison operation for respective variance values VAR(Y3) and VAR(Y4) is the same, equivalent or similar to the comparison operation of the second variance value VAR(Y2).

[0042] The comparator **240** may output an activity ACT corresponding to a determined variance value after a comparison operation for the sub-blocks SUB1 to SUB4 included in a current block is completed.

[0043] The variance register **260** may store a variance value VAR(Ym) that is transmitted from the comparator **240**, where m is one of natural numbers from 1 to 4.

[0044] An activity average decision circuit **300** may include at least an adder controller **320**, an adder **340**, an adder register **360**, and a division circuit **380**.

[0045] The adder controller **320** may transmit a control signal CTRL to the adder **340**. The adder controller **320** may